REMARKS

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested. Since the present Response raises no new issues, and in any event places the application in better condition for consideration on appeal, entry thereof is respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claim 1 to positively recite that the *first silicide regions have a lateral thickness from about 2 to about 15 nm which lowers external resistance of said device.* Support for this added feature to Claim 1 is found at paragraph [0045] of the originally filed specification as well as in cancelled Claim 16. Applicants submit that the previously added feature of forming a single p-dopant region within the substrate has been removed from the claim since the same is not needed to distinguish the claims from the art of record in this case. Although applicants have removed the feature of forming a single p-dopant region within the substrate from Claim 1, the present invention contemplates the possibility of forming the same.

Applicants submit that the above amendments to the claims were performed to better define applicants' claimed method and to distinguish the same from the art of record in the case, namely U.S. Patent No. 6,063,681 to Son, et al. Applicants observe that in the previous rejection the Examiner misinterpreted the thickness of the metal layer (100 to 200 Å, 10 to 20 nm) used in forming the first silicide as the thickness of the first silicide. The first silicide as reported at Col. 3, line 26 has a thickness from about 200 to 400 Å, i.e., 20 to 40 nm. Thus, Son, et al. require a first silicide that is thicker than the now claimed range of 2 to 15 nm for the purpose of preventing short channels in which an excess current flows that degrades device operation reliability. In the claimed

invention, the first silicide regions having a thickness from about 2 to about 15 nm lower the external resistance of the device. The external resistance of the device, as mentioned in paragraph [0004] of the present invention, is the sum of all of the resistance values except for the channel resistance. Note that the thicker the silicide, the lower the resistance the silicide is. Conversely, a thicker silicide provides for a high current interconnect. See paragraph [0007].

Minor amendments have been made to Claims 6, 7, 12, 18 and 19.

Since the above amendments to the claims do not introduce new matter into the specification and that the same do not raise any new issues, entry thereof is respectfully requested.

In the present Office Action, Claims 1, 6-9 and 11-19 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 6,063,681 to Son, et al. ("Son, et al.") and U.S. Patent No. 6,187,643 to Borland ("Borland"). Claims 2-3 stand rejected under 35 U.S.C. § 103 as allegedly obvious over the combined disclosures of Son, et al., Borland and U.S. Patent No. 6,313,020 to Kim, et al ("Kim, et al."). Claim 4 stands rejected under 35 U.S.C. § 103 as allegedly obvious over the combined disclosures of Son, et al., Borland, Kim, et al. and U.S. Patent No. 6,399,452 to Krishnan, et al. ("Krishnan, et al.").

Applicants respectfully submit that the combined disclosures of Son, et al. and Borland do not render the method recited in the claims of the present invention unpatentable since this combination does not teach or suggest the processing steps recited in Claim 1 of the present application. Specifically, the combined disclosures of Son, et al. and Borland do not teach or suggest a method for forming a low resistance MOSFET device which includes, among other processing steps, a step of forming first

silicide regions having a first silicide thickness in a substrate as well as atop a surface of a gate region, wherein the first silicide regions have a lateral thickness from about 2 to about 15 nm which lowers external resistance of said device.

The principal reference spurring the obviousness rejection, i.e., Son, et al., provides a semiconductor device (see FIG. 2) that includes a gate insulating film 24 and a gate electrode 25 formed on a prescribed region of a semiconductor substrate 21, sidewall spacers 26, 31 formed at both sides of the gate insulating film 24 and the gate electrode 25, first impurity regions 27 formed in surfaces of the semiconductor substrate 21 under the sidewall spacers 26, 31, second impurity regions 30 formed in the semiconductor substrate 21 on both sides of the sidewall spacers 26, 31 and the first impurity regions 27, first silicide films 29 at surfaces of the first impurity regions 27, and second silicide films 33 at surfaces of the gate electrode 25 and the second impurity regions 30. Applicants observe that in Son, et al. the first silicide films have a reported thickness, i.e., depth, from about 200 about 400 Å, i.e., 20 to 40 nm. As such, Son, et al. do not teach or suggest applicants' claimed method in which the first silicide having a thickness from about 2 to about 15 nm, which thickness is less than the thickness reported in Son, et al., is formed. The claimed thickness is said to reduce external resistance of the device, while the thickness reported in Son, et al. prevents short channels.

Borland does not alleviate the above defects in Son, et al. since the applied secondary reference also does not teach or suggest applicants' claimed step of forming first silicide regions having a first silicide thickness in a substrate as well as atop a surface of a gate region, wherein the first silicide regions have a lateral thickness from about 2 to about 15 nm which lowers external resistance of said device. Borland

provides a method of fabricating a circuit on a substrate. At col. 3, lines 61-62, Borland discloses that silicide contact 34 are formed atop the source/drain and gate electrode. No further details concerning the silicide contact formation is provided in Borland. Since no details of the silicide process are formed, it must be assumed that a conventional silicide process is used in which thick silicides, similar to that disclosed in Son, et al., are formed.

Based on the above remarks, the rejection to Claims 1, 6-9 and 11-19 under § 103 citing Son, et al. and Borland has been obviated. Reconsideration and withdrawal of the obviousness rejection citing Son, et al. and Borland are respectfully requested.

With respect to the rejection to Claims 2 and 3 under 35 U.S.C. § 103 citing the combined disclosures of Son, et al., Borland and Kim, et al., applicants respectfully submit that the foregoing combination is defective since the applied references do not teach or suggest applicants' claimed method recited in Claim 1. Specifically, the combined disclosures of Son, et al., Borland and Kim, et al do not teach or suggest applicants' claimed step of forming first silicide regions having a first silicide thickness in a substrate as well as atop a surface of a gate region, wherein the first silicide regions have a lateral thickness from about 2 to about 15 nm which lowers external resistance of said device.

Son, et al. and Borland are defective for the same reasons as discussed above. The defects in the combined disclosures of Son, et al. and Borland are not alleviate by Kim, et al. since that applied reference also does not teach or suggest applicants' claimed step of forming first silicide regions having a first silicide thickness in a substrate as well as atop a surface of a gate region, wherein the first silicide regions have a lateral thickness from about 2 to about 15 nm which lowers external resistance of said device.

In Kim, et al., silicide formation is discussed and conventional processes are used in forming the various silicide layers disclosed in Kim, et al. The applied reference does not provide specifics about the silicide formation and thus it must be assumed that a thick silicide, as disclosed in Son, et al., is formed since thick silicide formation is conventional and is state of the art.

Based on the above remarks, the rejection to Claims 2 and 3 under § 103 citing Son, et al., Borland and Kim, et al. has been obviated. Reconsideration and withdrawal of the obviousness rejection citing Son, et al., Borland and Kim, et al. are respectfully requested.

With respect to the rejection to Claim 4 under 35 U.S.C. § 103 citing the combined disclosures of Son, et al., Borland, Kim, et al. and Krishnan, et al., applicants respectfully submit that the foregoing combination is defective since the applied references do not teach or suggest applicants' claimed method recited in Claim 1. Specifically, the combined disclosures of Son, et al., Borland, Kim, et al. and Krishnan, et al. do not teach or suggest applicants' claimed step of forming first silicide regions having a first silicide thickness in a substrate as well as atop a surface of a gate region, wherein the first silicide regions have a lateral thickness from about 2 to about 15 nm which lowers external resistance of said device.

Son, et al., Borland and Kim, et al. are defective for the same reasons as discussed above. The defects in the combined disclosures of Son, et al., Borland and Kim, et al. are not alleviate by Krishnan, et al. since that applied reference also does not teach or suggest applicants' claimed step of forming first silicide regions having a first silicide thickness in a substrate as well as atop a surface of a gate region, wherein the

first silicide regions have a lateral thickness from about 2 to about 15 nm which lowers external resistance of said device.

In Krishnan, et al., silicide formation is discussed and a conventional process is used in forming the various silicide layers disclosed in Krishnan, et al. The applied reference does not provide specifics about the silicide layer and thus it must be assumed that a thick silicide, as disclosed in Son, et al., is formed since thick silicide formation is conventional and is state of the art.

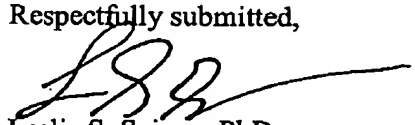
Based on the above remarks, the rejection to Claim 4 under § 103 citing Son, et al., Borland, Kim, et al. and Krishnan, et al. has been obviated. Reconsideration and withdrawal of the obviousness rejection citing Son, et al., Borland, Kim, et al. and Krishnan, et al. are respectfully requested.

The various § 103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed methods to include the various processing steps recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. § 103 have been obviated; therefore reconsideration and withdrawal thereof are respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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